CAPACITIVE PRESSURE SENSOR MOCK-UP WITHOUT COMPENSATION CIRCUITS

G. Blasquez*, P. Pons*, Ph. Ménini*, D. Herbst**, M. Schulz** and B. Höfflinger***

* CNRS/LAAS, 7 av. Roche, 31077 Toulouse, France
** Ht Mikroelektronik GmbH, Pappenstrasse 36, 47057 Duisburg, Germany
*** Institut für Mikroelektronik Stuttgart, Allmandring 30a, 7000 Stuttgart 80, Germany

ABSTRACT

A pressure sensor mock-up has been fabricated with an integrated capacitive pressure sensing cell and a CMOS switched capacitor circuit to evaluate the feasibility of sensors requiring no compensation circuits for the thermal drift and nonlinearities. The measurements made on this demonstrator and the analysis of potential improvements show that it must be possible to develop a sensor featuring : a linear response, an accuracy in the order of a few percents, a power consumption of 7.5 mW for a 5 V supply voltage.

1 - INTRODUCTION

Mass consumption markets require sensors that are both inexpensive and fairly accurate. To match these two contradictory requirements, the favorite solution consists of associating silicon piezoresistive sensors with temperature and offset voltage compensation circuits. The simplification or suppression of compensation operations would result in substantial savings. An evaluation made with capacitive devices [1] shows that this idea is not unrealistic if specifications indicates an accuracy between 2 to 5 percents.

In addition, capacitive devices offer other benefits. They consume little power and can be directly interfaced with switched-capacitor circuits. The design and fabrication of sensors comprising analog and digital functions on the same chip is easy.

In the sequel, a promising mock-up of pressure sensor is presented. It is based on the preceding considerations. Its development was made possible by the support of the European program EUREKA/PROMETHEUS. In its simplest form, it consists of two chips: a sensing cell and a CMOS electronic integrated circuit. Following the descriptions of the general architecture and preliminary characteristics, different improvements easily implementable are proposed.

2 - MOCK-UP DESCRIPTION

Figure 1 shows the construction of the demonstrator and the related wiring diagram.

The sensing cell has been designed and fabricated by LAAS. Its main features have been reported in [1]. Its structure is illustrated in figure 2. This is a dual variable capacitor whose diaphragm is made of Silicon. The Pyrex substrate holds two concentric fixed plates. The inner plate, together with the diaphragm, forms the measurement capacitor (denoted C_m in Fig. 1). The outer plate, together with the diaphragm edges, constitutes a pseudo reference capacitor C_r. At rest, $C_m \approx C_r \approx 25$ pF. The sensitivity to pressure of C_m is of the order of 1pF/bar. The role of C_r is to compensate for the initial value of C_m.

Via the capacitors C_s, C_r and C_m are connected to the two inputs of a differential capacitance/voltage converter (KASIS) designed by Ht Mikroelecktronik GmbH and manufactured by IMS Stuttgart. The table gives a brief overview of the characteristics of this integrated circuit.

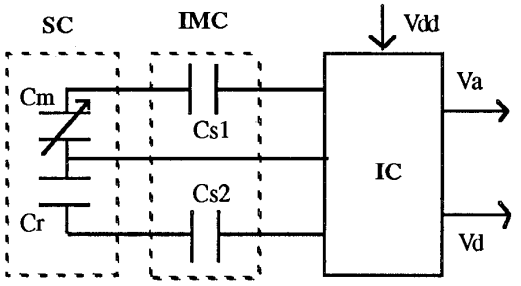

Fig. 1 : Demonstrator architecture. SC : Sensing Cell; IMC : Impedance Matching Capacitors; IC : Integrated Circuit; Vdd : Supply Voltage; Va and Vd Analog and Digital Outputs respectively

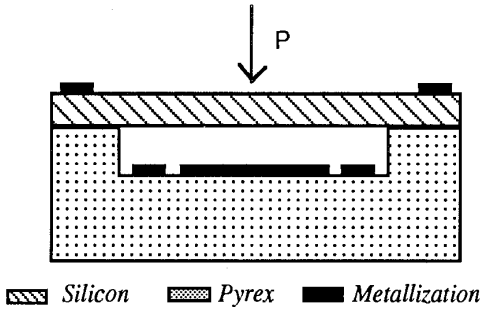

Fig. 2 : Sensing cell structure (Pa: Applied Pressure)

Let V_a be the analog output, V_{dd} the supply voltage and C_f a feedback capacitor integrated into the circuit. In theory, the converter's response can be expressed as follows:

$$V_a \cong \frac{V_{dd}}{2} + \frac{\Delta C}{C_f} \qquad (1)$$

where ΔC is the difference between the two capacitances seen by the two inputs. The capacitance of C_f is in the order of 10 pF. Connecting in series C_{s1} with C_m and C_{s2} with C_r allows the adjustement of the offset voltage and the range of the measurement scale. C_{s1}, C_{s2}, C_m and C_r are linked to ΔC by the formula:

$$\Delta C = \frac{C_{s1}\, C_m}{C_{s1} + C_m} - \frac{C_{s2}\, C_r}{C_{s2} + C_r} \qquad (2)$$

Chip size	16.5 mm2
Technology	3 µm CMOS p well
Supply voltage Vdd	3 to 5.3 V
Power consumption (Vdd=5V)	7.5 mW
Operating temperature range	- 40 °C to 90 °C
Input range (low sensitivity)	± 2.4 pF
Input range (high sensitivity)	± 0.6 pF
Digital output	8 bits + sign
Analog output	9 bits

Table : Succint features of the integrated interface for capacitive sensors (KASIS)

3 - EXPERIMENTAL RESULTS

Preliminary evaluation tests have been carried out from 1 to 6 bars and between -10°C and 90°C.

Figure 3 shows an example of response measured in the following conditions: V_{dd} = 5V, T = 30°C, $C_{s1} = C_{s2}$ = 45 pF. The dots represent the measurements. As a first approximation, the response is of the linear type (represented by the solid line in figure 3) with an offset voltage Vo = 2.7 V and a pressure sensitivity S = 0.268 V/bar.

If E(P) denotes the difference between the measurements and the linear model, the response can be expressed analytically by the equation :

$$V_a(P) = Vo + SP + E(P) \qquad (3)$$

Nonlinearity errors are specified in figure 4. They are characterized by the parameter NL defined by the expression:

$$NL = \frac{100 \times E(P)}{V_a(6) - V_a(1)} \qquad (4)$$

In figure 4 it appears that the nonlinearity error (NL) is less than or equal to ± 2.5 percents of the full scale.

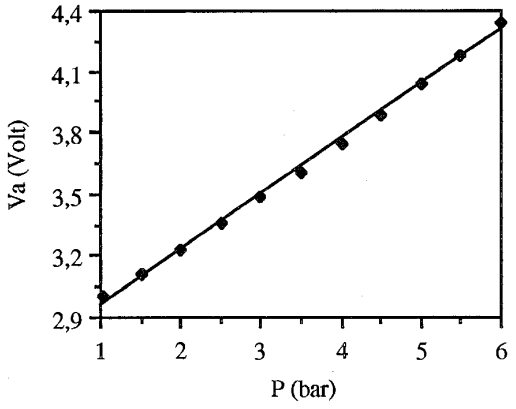

Fig 3: Mock-up response between 1 to 6 bars (T=30°C)

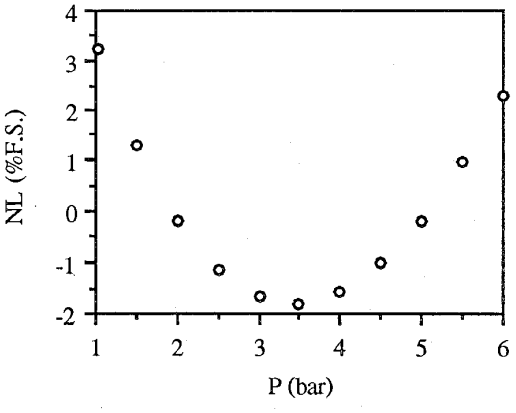

Fig 4 : Mock-up nonlinearity (T=30°C)

Figures 5 to 7 show the influence of temperature on the responses, the offset voltage and the pressure sensitivity. Computation of the thermal coefficient of pressure sensitivity yields a TCS in the order of 200 ppm/°C. Interestingly, the drifts of Vo and S are highly correlated.

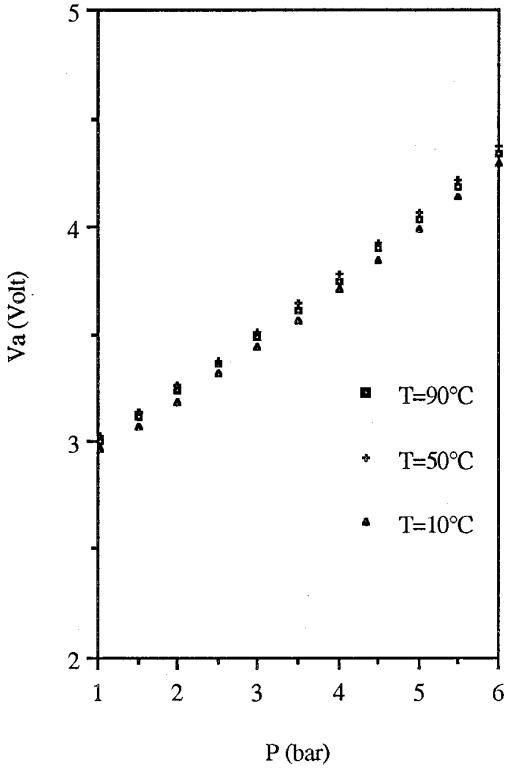

Fig 5 : Influence of the temperature on the response

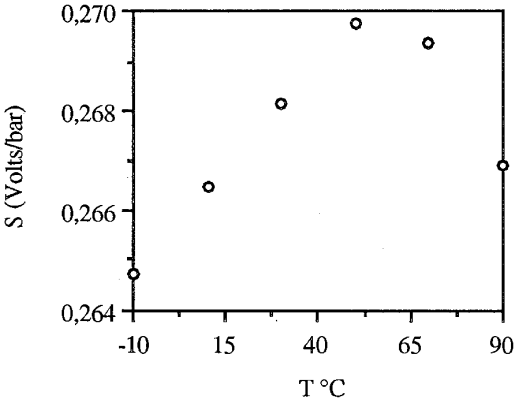

Fig 6 : Pressure sensitivity drift vs. temperature

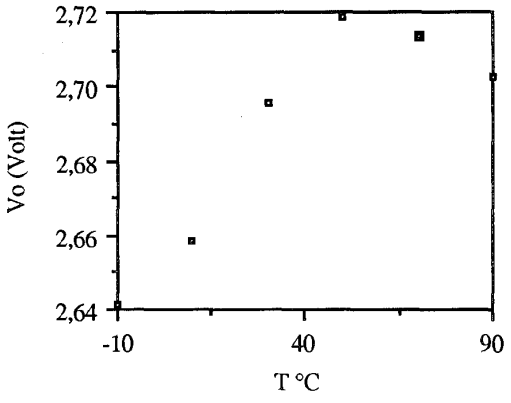

Fig 7 : Offset drift vs. temperature

Finally the operation of the mock-up is not disturbed if capacitors less than or equal to 100 pF are connected between the silicon plate and the ground. In our experiments, they simulate parasitic capacitors between the silicon plate and the package or the circuits inputs and the ground. The high value of the parasitic capacitances tolerated by the mock-up suggests that a large variety of packages can be employed to fabricate sensors.

4 - FUTURE PROSPECTS

The data presented here cannot be considered as fully representative of the mock-up's ultimates potentialities. First it is worth pointing out that the temperature range in which the sensor can operate is not limited to -10°C. Indeed, the sensing cell and the converter can be operated down to - 40°C. The actual limit originates from their mockup packaging that has not been optimized in order to avoid humidity condensation effects. This is a well-known problem that has been adequately addressed by packaging experts.

Also, the mock-up can be operated at pressures less than 1 bar and higher than 6 bars. The pressure causing the plates to come into contact is around 20 bars [2]. Consequently by properly selecting the capacitances C_S and/or by shifting Vo, the measurement range can be extended or shifted, and the pressure sensitivity can be increased or decreased.

With respect to nonlinearity errors, the optimization of the form and size of the fixed plates should lead to errors less than or equal to 1 %. Also the temperature influence can be significantly compensated for by judiciously varying V_{dd}.

Note that the integration of the capacitors C_S into the sensing cell or the converter reduces the total number of devices from four to two. Lastly, the mock-up can be equipped with a self-test function by integrating in parallel with C_r and C_m switchable auxiliary capacitors which simulate pressure variations.

REFERENCES

[1] P. Pons, G. Blasquez, R. Behocaray
Sensors and Actuators - A, 37-38 (1993) pp 112-115
Feasibility of capacitive pressure sensor without compensation circuit

[2] X. Chauffleur, G. Blasquez and P. Pons
Eurosensors VIII Conference, Toulouse 25-28 Sept. 1994
Influence of the bonding conditions on the response of capacitive pressure sensors